SONY

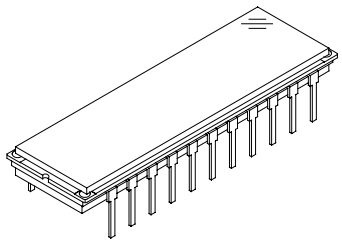
ILX570K

5340-pixel × 6 line CCD Linear Sensor (Color)

Description

The ILX570K is a reduction type CCD linear sensor developed for color image scanner. This sensor reads A4-size documents at a density of 1200 DPI.

22 pin DIP (Plastic)



Sensor Line Features

- Number of effective pixels:
  32040 pixels (5340 pixels × 6)
- Pixel size: 4µm × 4µm (4µm pitch)
- Distance between main lines: 48µm (12 lines)
- Distance between main line and sub line: 8µm (2 lines)

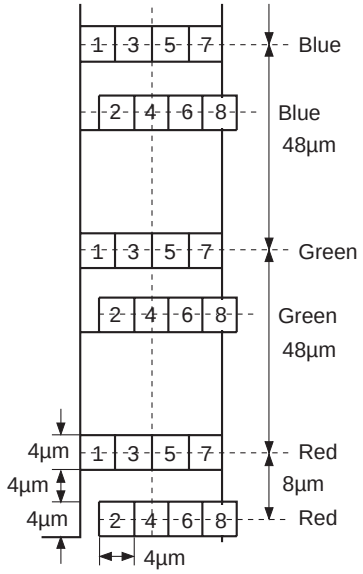
Common Features

- Single-sided readout
- Ultra low lag
- Single 12V power supply
- Maximum data rate: 10MHz/Color
- Input clock pulse: CMOS 5V drive
- Number of output: 3 (R, G, B)
- Package: 22-pin Plastic DIP (400mil)

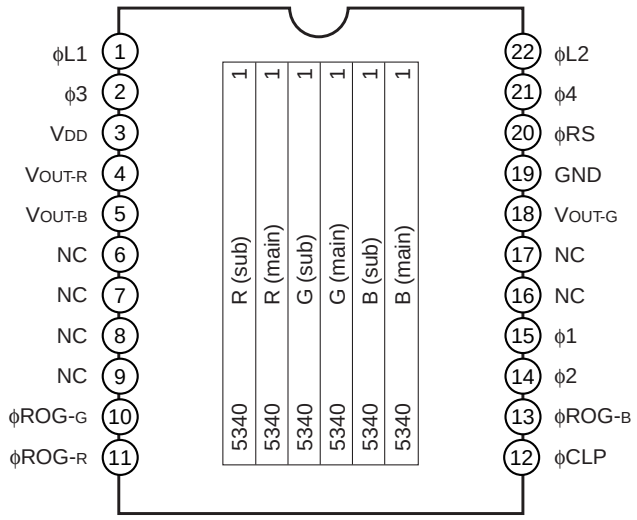
Absolute Maximum Ratings

• Supply voltage	V_{DD}	15	V
• Operating temperature		–10 to +55	°C

Sensor Configuration



Pin Configuration (Top View)



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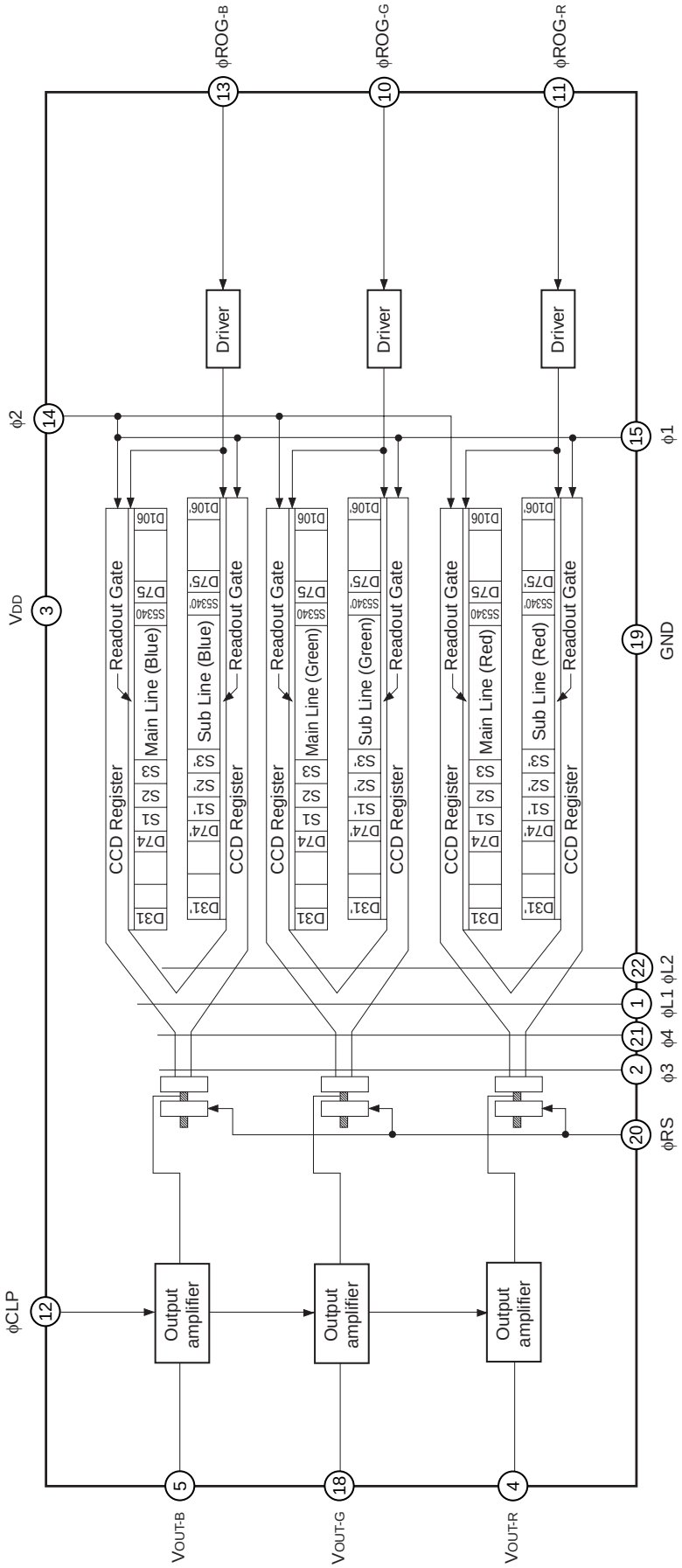
Block Diagram



Pin Description

Pin No.	Symbol	Description	Pin No.	Symbol	Description
1	φL1	Clock pulse input	12	φCLP	Clock pulse input
2	φ3	Clock pulse input	13	φROG-B	Clock pulse input
3	V_{DD}	12V power supply	14	φ2	Clock pulse input
4	V_{OUT-R}	Signal output (red)	15	φ1	Clock pulse input
5	V_{OUT-B}	Signal output (blue)	16	NC	NC
6	NC	NC	17	NC	NC
7	NC	NC	18	V_{OUT-G}	Signal output (green)
8	NC	NC	19	GND	GND
9	NC	NC	20	φRS	Clock pulse input
10	φROG-G	Clock pulse input	21	φ4	Clock pulse input
11	φROG-R	Clock pulse input	22	φL2	Clock pulse input

Recommended Supply Voltage

Item	Min.	Typ.	Max.	Unit
V_{DD}	11.4	12	12.6	V

Clock Characteristics

Item	Symbol	Min.	Typ.	Max.	Unit
Input capacity of φ1, φ2	$C_{\phi 1}$, $C_{\phi 2}$	—	1100	—	pF
Input capacity of φRS	$C_{\phi RS}$	—	10	—	pF
Input capacity of φCLP	$C_{\phi CLP}$	—	10	—	pF
Input capacity of φROG	$C_{\phi ROG}$	—	10	—	pF
Input capacity of φ3, φ4, φL1, φL2	$C_{\phi L1}$, $C_{\phi L2}$, $C_{\phi 3}$, $C_{\phi 4}$	—	20	—	pF

Clock Frequency

Item	Symbol	Min.	Typ.	Max.	Unit
φ1, φ2, φL1, φL2	$f_{\phi 1}$, $f_{\phi 2}$, $f_{\phi L1}$, $f_{\phi L2}$	—	0.5	8	MHz
φ3, φ4, φRS	$f_{\phi 3}$, $f_{\phi 4}$, $f_{\phi RS}$	—	1	10	MHz

Input Clock Pulse Voltage Condition

Item		Min.	Typ.	Max.	Unit
φ1, φ2, φRS, φROG, φL1, φL2, φ3, φ4, φCLP pulse voltage	High level	4.75	5.0	5.25	V
	Low level	—	0	0.1	V

Electro-optical Characteristics (Note 1)

(Ta = 25°C, V_{DD} = 12V, $f\phi_{RS}$ = 1MHz, Input clock = 5Vp-p, Light source = 3200K, IR cut filter CM-500S (t = 1.0mm))

Item		Symbol	Min.	Typ.	Max.	Unit	Remarks
Sensitivity	Red	R_R	3.1	4.4	5.0	V/(lx · s)	Note 2
	Green	R_G	4.4	6.3	8.2		
	Blue	R_B	3.0	4.3	5.6		
Sensitivity nonuniformity		PRNU	—	4.0	20	%	Note 3
Saturation output voltage		V_{SAT}	2.1	2.5	—	V	Note 4
Saturation exposure	Red	SE_R	—	0.57	—	lx · s	Note 5
	Green	SE_G	—	0.40	—		
	Blue	SE_B	—	0.58	—		
Dark voltage average		V_{DRK}	—	2.0	5.0	mV	Note 6
Dark signal nonuniformity		DSNU	—	4.0	12	mV	
Image lag		IL	—	0.02	—	%	Note 7
Supply current		I_{VDD}	—	30	50	mA	Note 8
Total transfer efficiency		TTE	92	98	—	%	
Output impedance		Z_O	—	260	—	Ω	
Offset level		V_{OS}	—	5.5	—	V	Note 9

Notes:

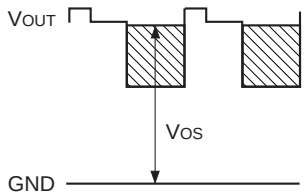
1. In accordance with the given electro-optical characteristics, the black level of 1200 DPI is defined as the average value of D32, D33 to D73.
2. For the sensitivity test, light is applied with a uniform intensity of illumination.
3. PRNU is defined as indicated below. Ray incidence conditions are the same as for Note 2.
   V_{OUT} = 500mV (typ.)

$$PRNU = \frac{(V_{MAX} - V_{MIN})/2}{V_{AVE}} \times 100\ [\%]$$

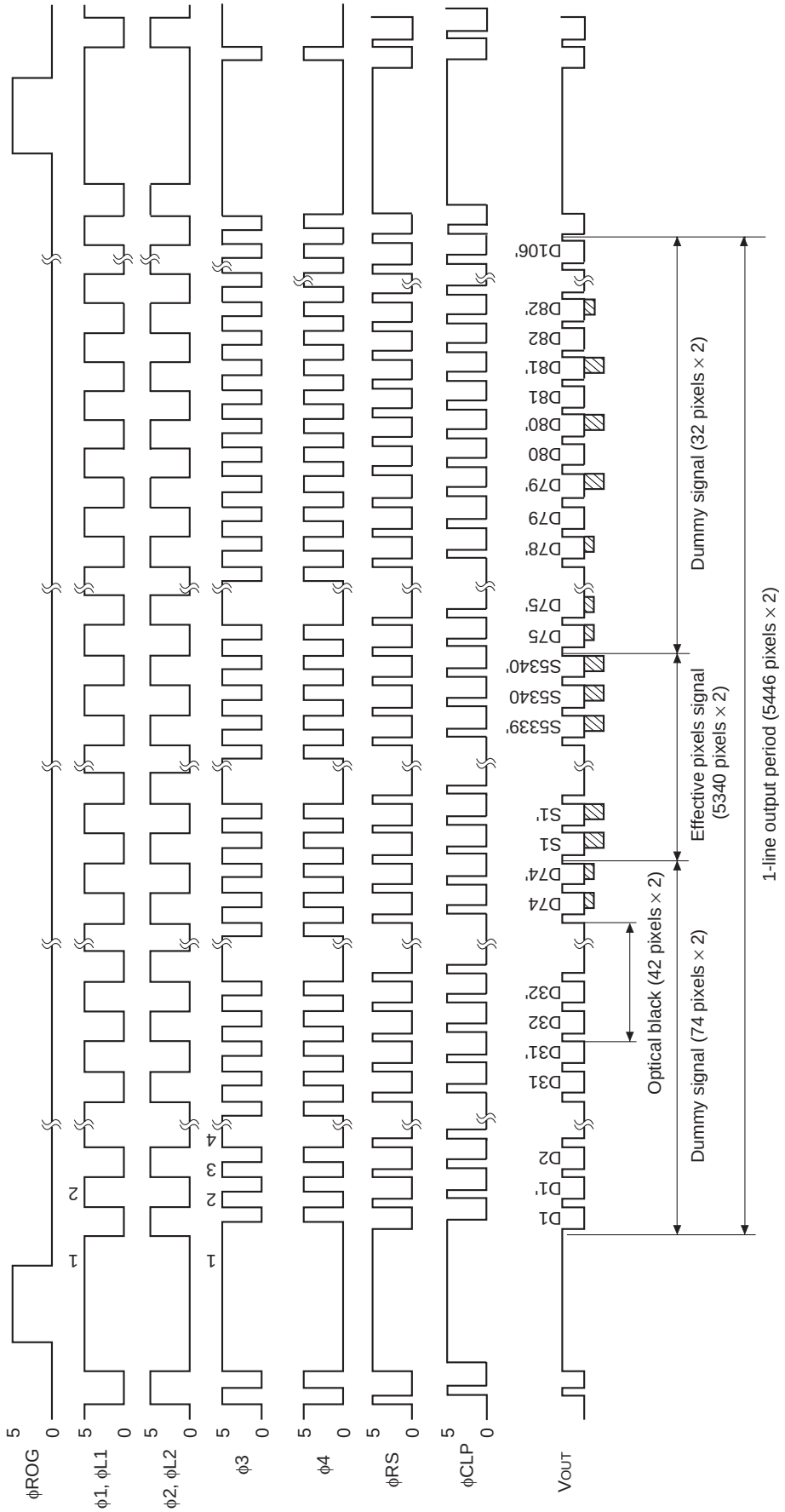
4. Use below the minimum value of the saturation output voltage.
5. Saturation exposure is defined as follows.

$$SE = \frac{V_{SAT}}{R}$$

   Where R indicates R_R, R_G, R_B and SE indicates SE_R, SE_G, SE_B.
6. Optical signal accumulated time τint stands at 5.5ms.
7. V_{OUT-G} = 500mV (typ.)
8. Supply current means the total current of this device.
9. Vos is defined as indicated below.
   V_{OUT} indicates V_{OUT-R}, V_{OUT-G}, and V_{OUT-B}.

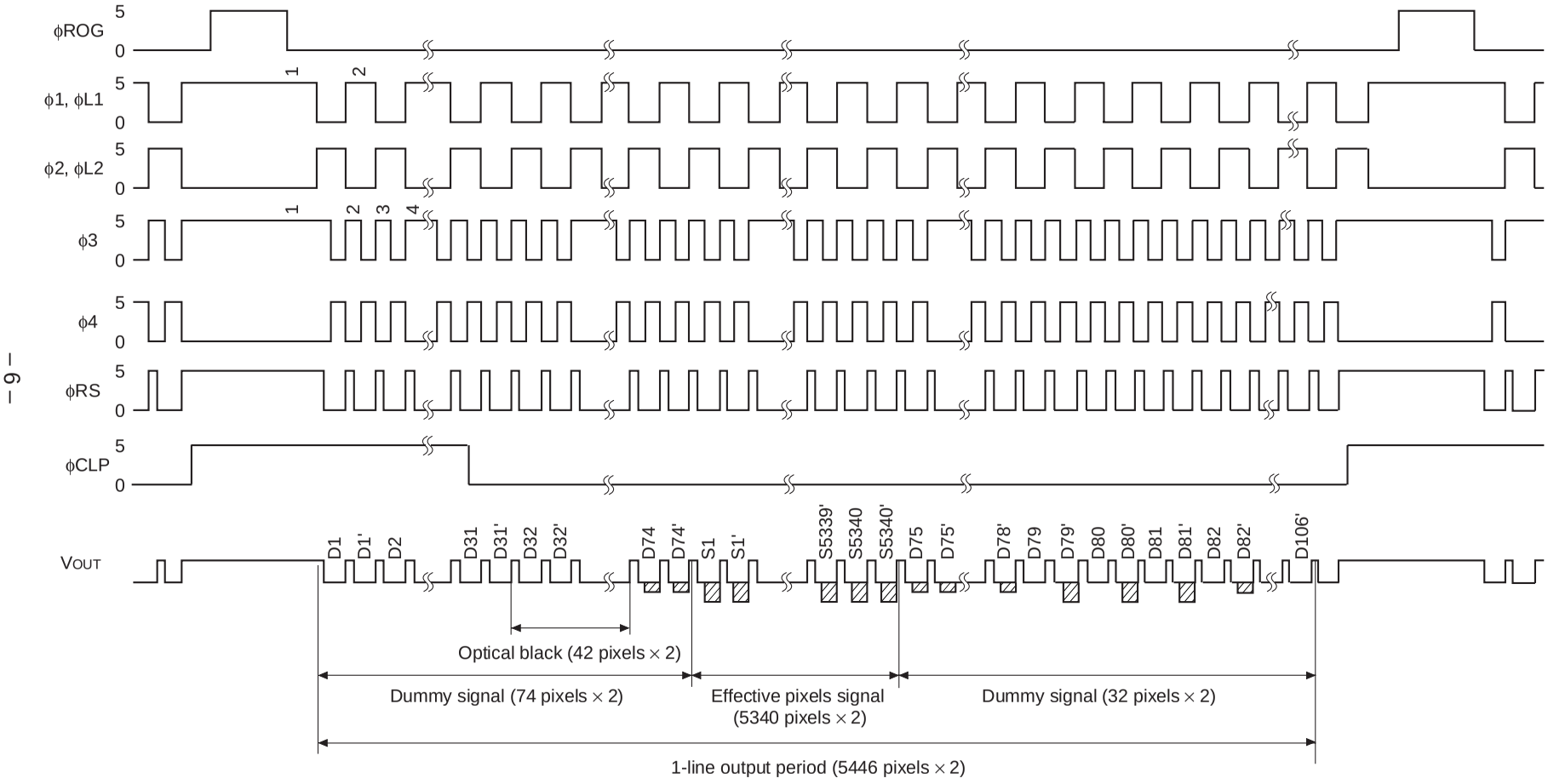


Clock Timing Chart 1 1200 DPI Staggered (pixel clamp mode)



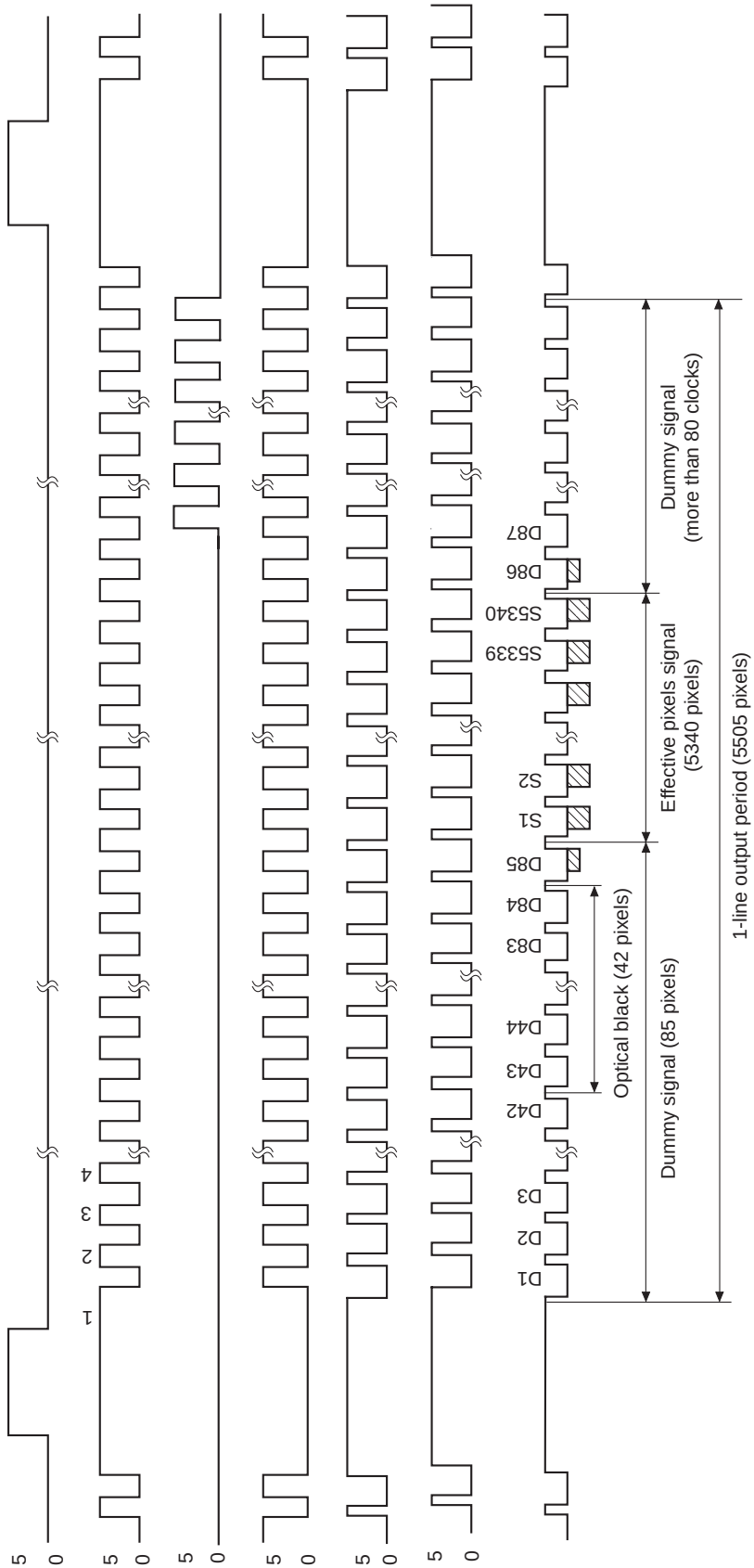
Note) The transfer pulses (φ1, φ2) must have more than 5446 cycles.
The transfer pulses (φ3, φ4) must have more than 10892 cycles.
V_{OUT} indicates V_{OUT-R}, V_{OUT-G}, V_{OUT-B}.

Clock Timing Chart 2 1200 DPI Staggered (line clamp bode)



Note) The transfer pulses (φ1, φ2) must have more than 5446 cycles.
The transfer pulses (φ3, φ4) must have more than 10892 cycles.
VOUT indicates VOUT-R, VOUT-G, VOUT-B.

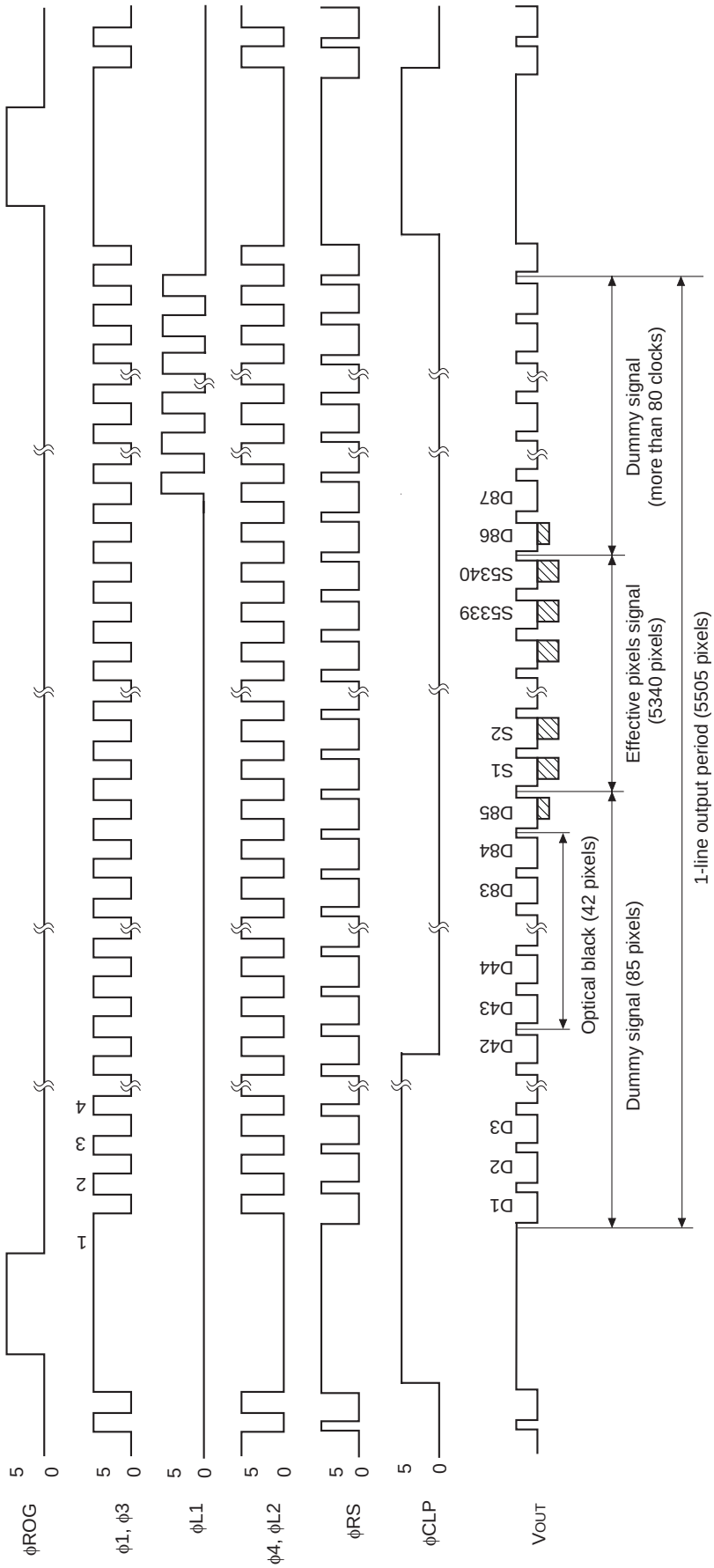
Clock Timing Chart 3 600 DPI Staggered (pixel clamp bode)



Note) The transfer pulses (φ1, φ2) must have more than 5505 cycles.

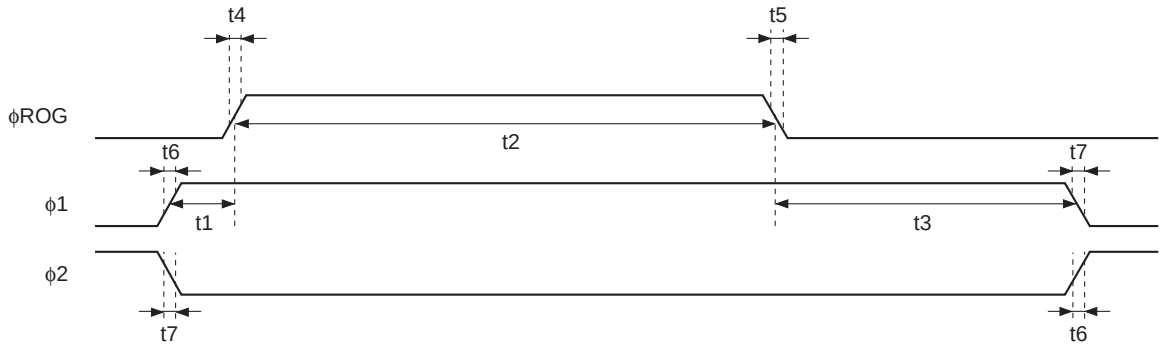
VOUT indicates VOUT-R, VOUT-G, VOUT-B.

Clock Timing Chart 4 600 DPI Staggered (line clamp bode)

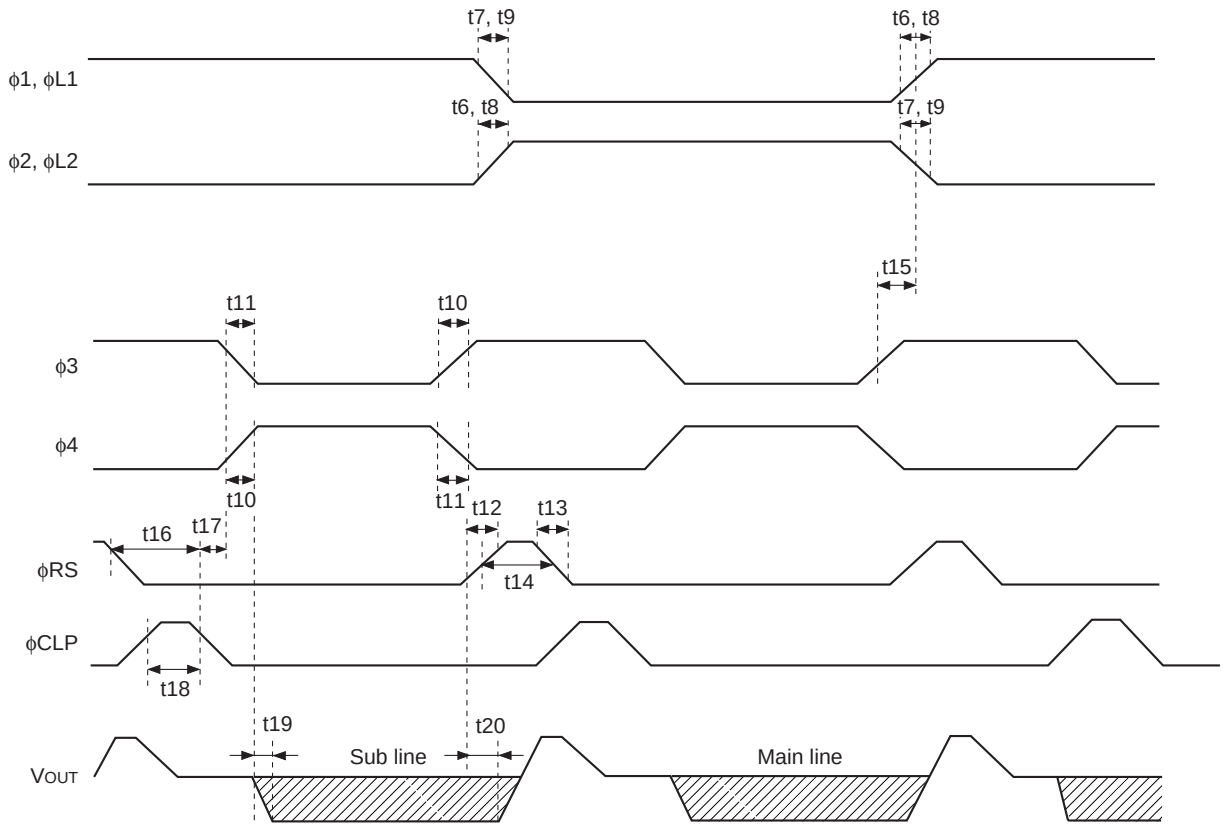


Note) The transfer pulses (φ1, φ2) must have more than 5505 cycles.
VOUT indicates VOUT-R, VOUT-G, VOUT-B.

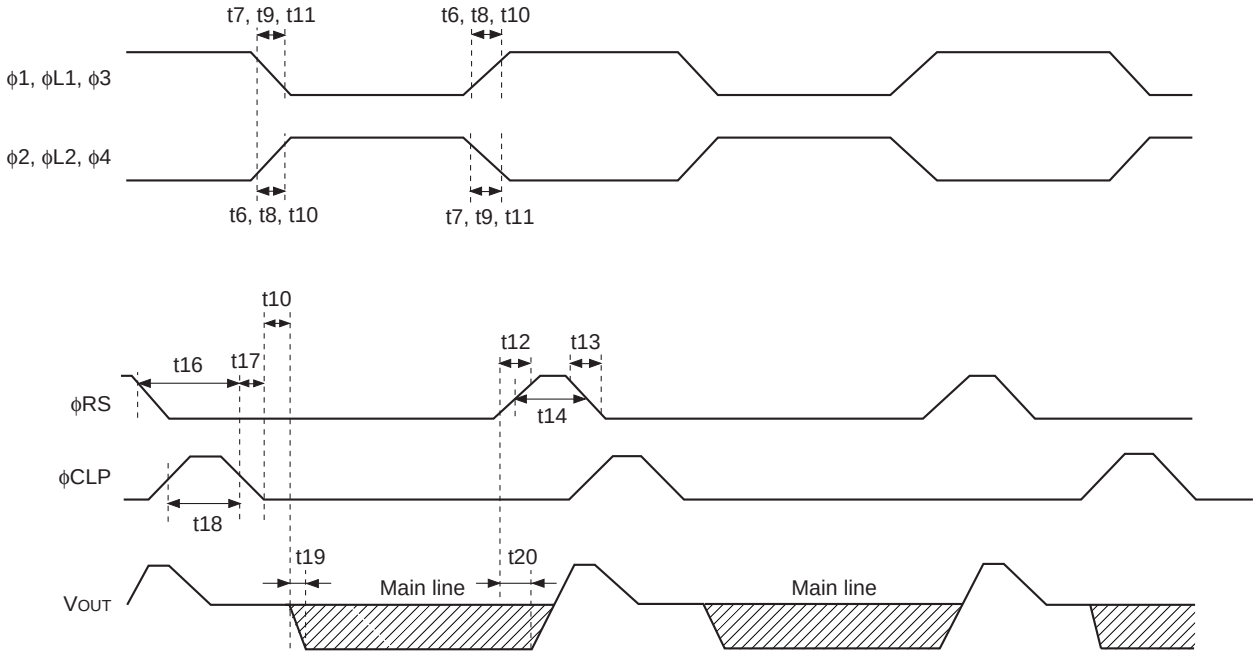
Clock Timing Chart 5 1200 DPI Staggered and 600 DPI Linear



Clock Timing Chart 6 (1200 DPI pixel mode)



ClockTiming Chart 7 (600 DPI pixel mode)

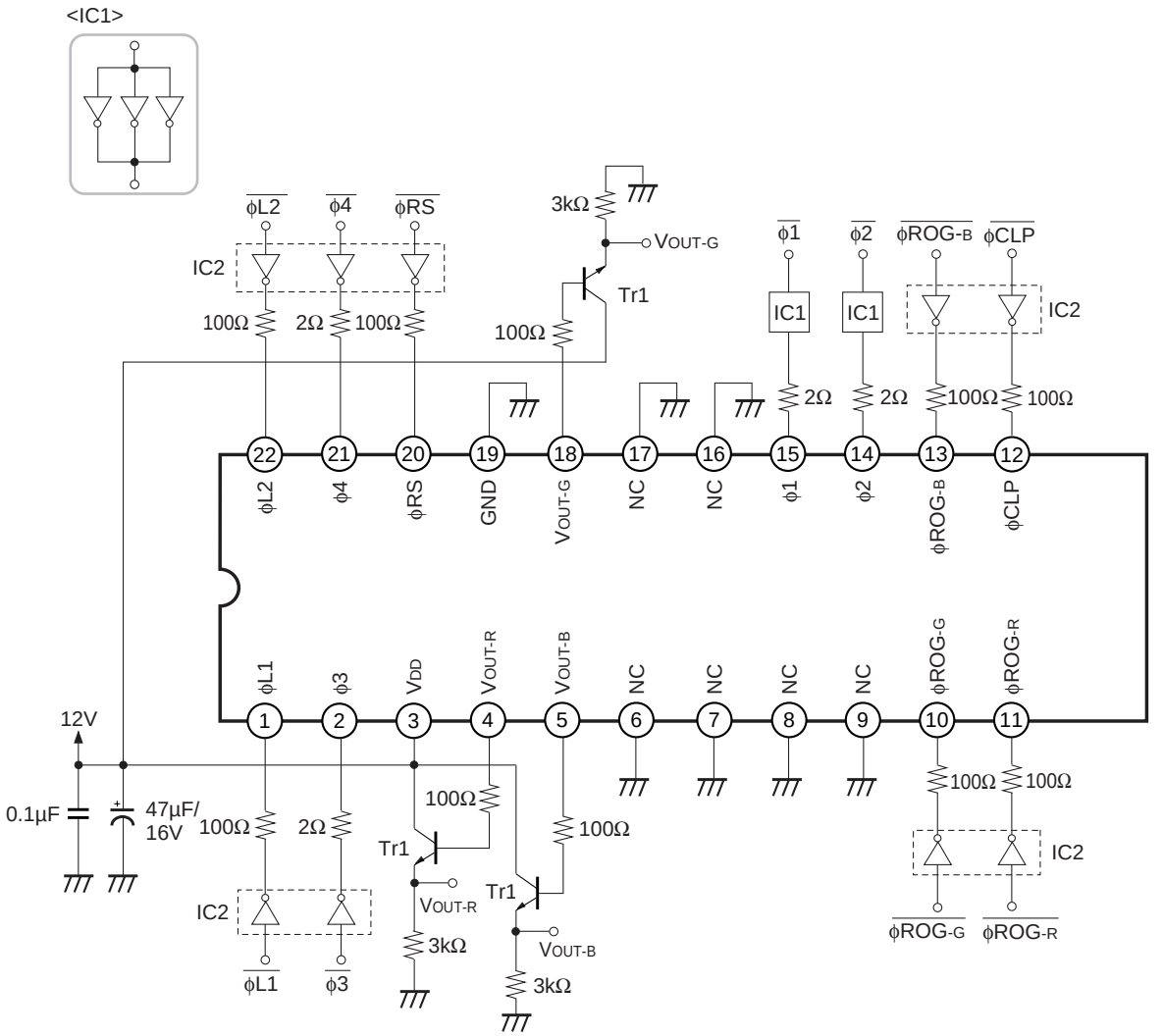


Clock Pulse Recommended Timing

Item	Symbol	Min.	Typ.	Max.	Unit
φROG, φ1 pulse timing	t1	50	100	—	ns
φROG pulse high level period	t2	5000	6000	—	ns
φROG, φ1 pulse timing	t3	1200	1500	—	ns
φROG pulse rise time	t4	0	5	10	ns
φROG pulse fall time	t5	0	5	10	ns
φ1, φ2.pulse rise time	t6	0	50	80	ns
φ1, φ2.pulse fall time	t7	0	50	80	ns
φL1, φL2 pulse rise time	t8	0	10	30	ns
φL1, φL2 pulse fall time	t9	0	10	30	ns
φ3, φ4 pulse rise time	t10	0	10	30	ns
φ3, φ4 pulse fall time	t11	0	10	30	ns
φRS pulse rise time	t12	0	10	30	ns
φRS pulse fall time	t13	0	10	30	ns
φRS pulse high level period	t14	30	100*1	—	ns
φL1, φL2 and φ3 pulse timing	t15	0	10	—	ns
φRS, φCLP pulse timing	t16	10	100	—	ns
φCLP, φL1, φ3 pulse timing	t17	5	100	—	ns
φCLP pulse high level period	t18	30	100	—	ns
Signal output delay time	t19	—	50	—	ns
	t20	—	20	—	ns

*1 These timing data is the recommended condition under $f_{\phi RS}$ = 1MHz.

Application Circuit*1

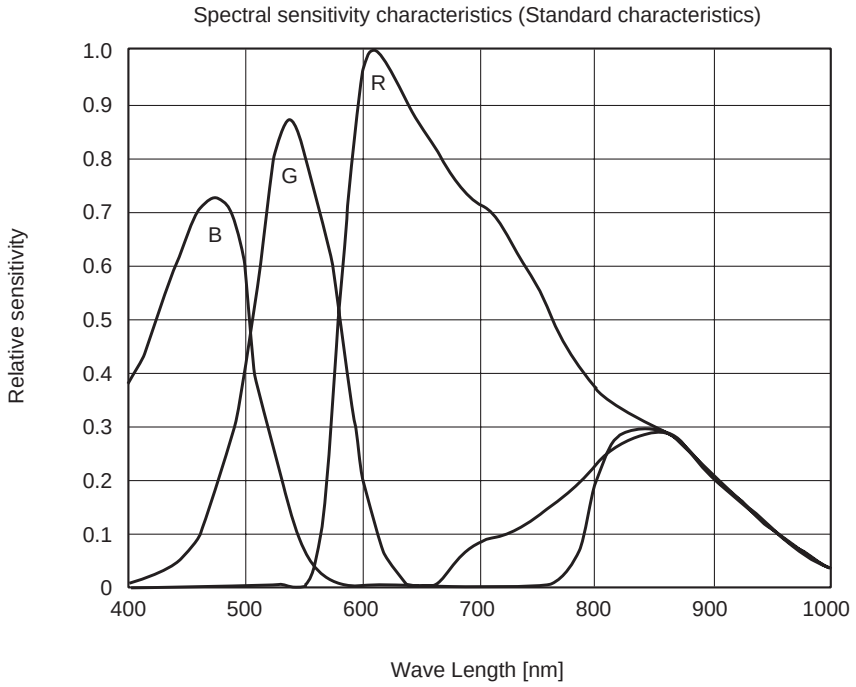


*1 Data rate $f_{\phi RS}$ = 1MHz

IC1: 74AC04 × 3pcs
IC2: 74HC04
Tr1: 2SC1815 - Y

Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Example of Representative Characteristics (V_{DD} = 12V, Ta = 25°C)



Notes on Handling

1. Static charge prevention

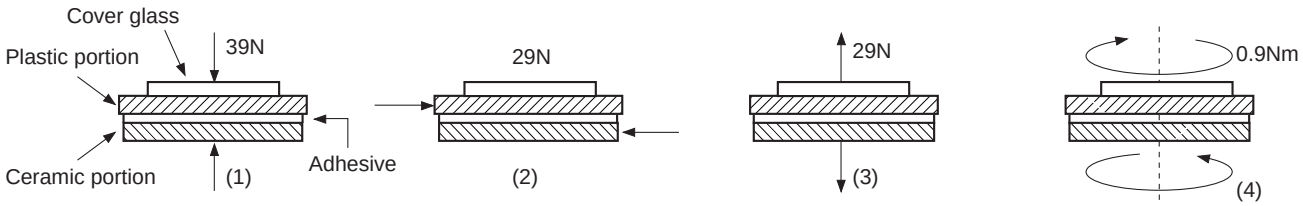
   CCD image sensors are easily damaged by static discharge. Before handling be sure to take the following protective measures.

   a) Either handle bare handed or use non-chargeable gloves, clothes or material.
      Also use conductive shoes.
   b) When handling directly use an earth band.
   c) Install a conductive mat on the floor or working table to prevent the generation of static electricity.
   d) Ionized air is recommended for discharge when handling CCD image sensors.
   e) For the shipment of mounted substrates, use boxes treated for the prevention of static charges.

2. Notes on handling CCD packages

   The following points should be observed when handling and installing packages.

   a) Remain within the following limits when applying a static load to the package.
      (1) Compressive strength: 39N/surface (Do not apply load more than 0.7mm inside the outer perimeter of the glass portion.)
      (2) Shearing strength: 29N/surface
      (3) Tensile strength: 29N/surface
      (4) Torsional strength: 0.9Nm



   b) In addition, if a load is applied to the entire surface by a hard component, bending stress may be generated and the package may fracture, etc., depending on the flatness of the ceramic portion. Therefore, for installation, either use an elastic load, such as a spring plate, or an adhesive.
   c) Be aware that any of the following can cause the packege to crack or dust to be generated.
      (1) Applying repetitive bending stress to the external leads.
      (2) Applying heat to the external leads for an extended period of time with soldering iron.
      (3) Rapid cooling or heating.
      (4) Prying the plastic portion and ceramic portion away at a support point of the adhesive layer.
      (5) Applying the metal a crash or a rub against the plastic portion.
      Note that the preceding notes should also be observed when removing a component from a board after it has already been soldered.
   d) The notch of the plastic portion is used for directional index, and that can not be used for reference of fixing. In addition, the cover glass and seal resin may overlap with the notch or ceramic may overlap with the notch of the plastic portion.

3. Soldering
   a) Make sure the package temperature does not exceed 80°C.
   b) Solder dipping in a mounting furnance causes damage to the glass and other defects. Use a 30W soldering iron with a ground wire and solder each pin in less than 2 seconds. For repairs and remount, cool sufficiently.
   c) To dismount an image device, do not use a solder suction equipment. When using an electric desoldering tool, ground the controller. For the control system, use a zero-cross type.

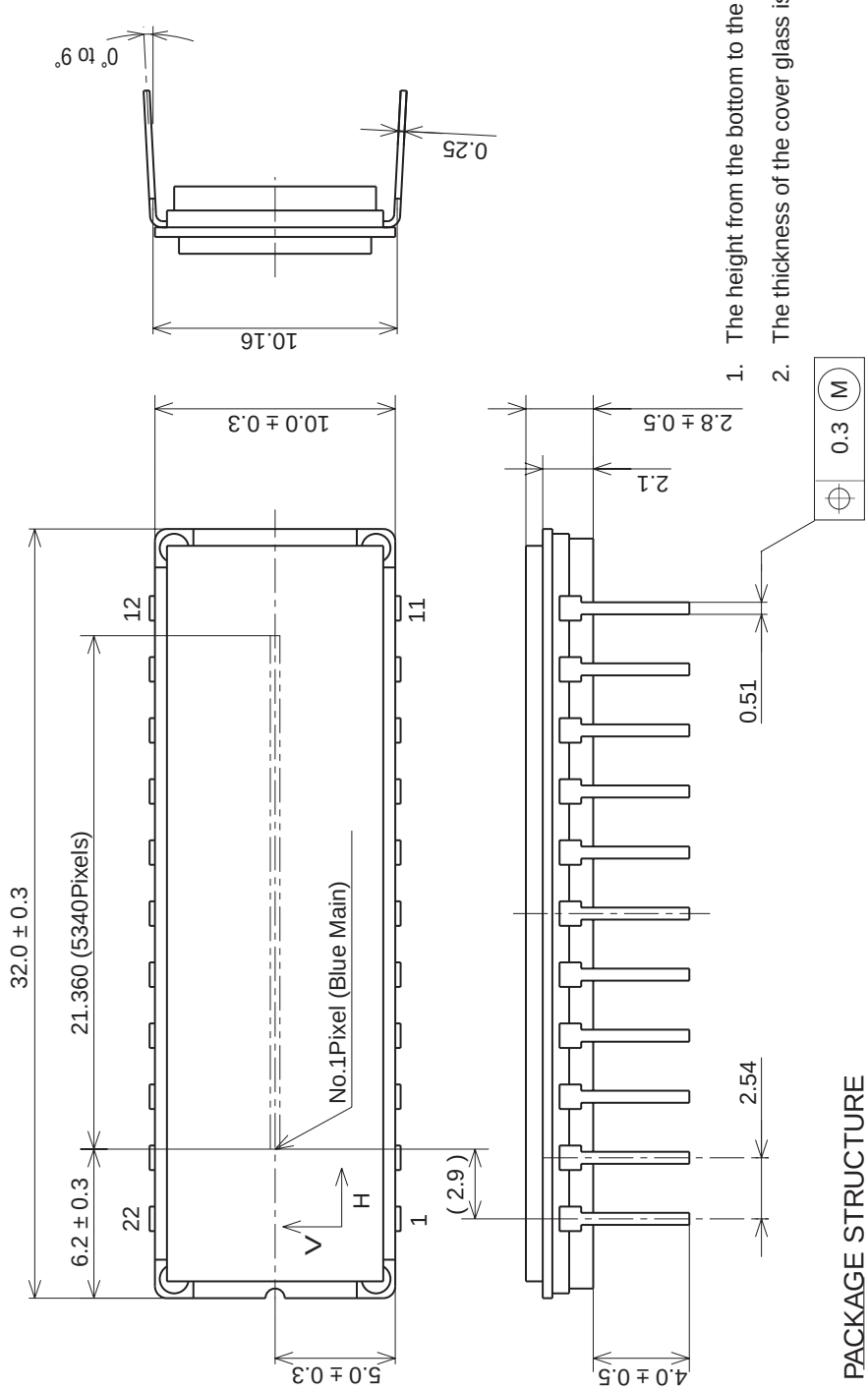
4. Dust and dirt protection
   a) Operate in clean environments.
   b) Do not either touch glass plates by hand or have any object come in contact with glass surfaces. Should dirt stick to a glass surface, blow it off with an air blower. (For dirt stuck through static electricity, ionized air is recommended.)
   c) Clean with a cotton bud and ethyl alcohol if the glass surface is grease stained. Be careful not to scratch the glass.
   d) Keep in a case to protect from dust and dirt. To prevent dew condensation, preheat or precool when moving to a room with great temperature differences.

5. Exposure to high temperatures or humidity will affect the characteristics. Accordingly avoid storage or usage in such conditions.

6. CCD image sensors are precise optical device that should not be subject to mechanical shocks.

Package Outline Unit: mm

22pin DIP (400mil)



1. The height from the bottom to the sensor surface is 1.61 ± 0.3mm.
2. The thickness of the cover glass is 0.7mm, and the refractive index is 1.5.

PACKAGE STRUCTURE

PACKAGE MATERIAL	Plastic,Ceramic
LEAD TREATMENT	GOLD PLATING
LEAD MATERIAL	42 ALLOY
PACKAGE MASS	2.21g
DRAWING NUMBER	LS-D18(E)